## REMARKS

Claims 1-4 are withdrawn. Claims 5, 6, and 13 are amended to address the 35 U.S.C. § 112 issues identified by the Examiner. Claims 5-13 remain in the Application. Reconsideration of the pending claims is respectfully requested in view of the above amendment and the following remarks.

## I. Claims Rejected Under 35 U.S.C. § 112

Claims 5-13 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claims 5, 6, and 13 are rejected because of insufficient antecedent basis for some of the claimed elements. Applicants amend Claim 5 to replace "the second gate insulator layer" with "a second insulator layer," amend Claim 6 to recite "the first gate insulator layer" and "the second insulator layer," and amend Claim 13 to recite "the first gate insulator layer." Approval of the amendment is respectfully requested.

## II. Claims Rejected Under 35 U.S.C. § 103(a)

A. Claims 5, 12, and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhodes (U.S. Pre-Grant Publication No. 2001/0012225) in view of El Gamal et al. (U.S. Patent No. 6,642,543) and Huang et al. (U.S. Patent No. 6,146,795). Applicants respectfully traverse the rejection.

To establish a *prima facie* case of obviousness, the relied upon references must teach or suggest every limitation of the claim such that the invention as a whole would have been obvious at the time the invention was made to one skilled in the art. Among other elements, amended Clam 5 recites:

> "a).... a pixel array having a number of pixels, each pixel containing a drive transistor, a select transistor, a transfer transistor and a reset transistor;....
>
> g) forming a plurality of photodiodes and a plurality of the drive transistors, the select transistors, the transfer transistors and the reset transistors in the pixel array based on the first and the second gate insulator layers and at least one transistor in the logic circuit based on the second gate insulator layer."

Applicants submit that none of the cited references teach or suggest these elements.

The Examiner recognizes that Rhodes fails to disclose basing the pixel transistors on the first gate insulator layer, but relies on El Gamal to remedy the defect. Rhodes discloses an image sensor having a pixel 14 containing a drive transistor 36, a select transistor 38, a transfer transistor 28, and a reset transistor 32. Rhodes also discloses a readout circuit 60 which may be characterized as the logic circuit. However, Rhodes does not disclose any transistors having dual gate insulator layers. All of the transistors disclosed by Rhodes, including the transistors in the pixel and the logic circuit, are based on a gate insulator layer having the same thickness.

El Gamal does not cure the defect of Rhodes. El Gamal discloses an image sensor having a pixel containing a reset transistor 520, a drive transistor 510, and a select transistor 540, wherein each gate of the reset transistor 520 and the drive transistor 510 is thicker than that of the select transistor 540. Thus, El Gamal at most discloses a pixel having transistors of two different thicknesses.

Accordingly, combining the teaching of Rhodes and El Gamal, a person of skill in the art would at most produce an image sensor including a pixel array that has transistors of two different thicknesses. Even assuming for the sake of argument that such image sensor has each of the claimed transistors (e.g., a drive transistor, a select transistor, a transfer transistor, a reset transistor, and at least one transistor in a logic circuit), the image sensor would not have all of the transistors in the pixel array of one thickness and the transistors in the logic circuit of another thickness. That is, the combined image sensor would at most include a pixel array with each of a drive transistor, a transfer transistor and a reset transistor 32 having a first gate insulator layer, and a select transistor 38 (which is also part of the pixel array) having a second gate insulator layer, wherein a thickness of the first gate insulator layer is higher than that of the second gate insulator layer. The cited references do not, separately or combined, teach or suggest that the transistors in the logic circuit have a different thickness from the transistors in the pixel array.

By contrast, the method of Claim 5 requires that all of the transistors in the pixel array have the first and the second gate insulator layers and at least one transistor in the logic circuit has the second gate insulator layer. None of the cited references, separately or combined, teach

or suggest all of these limitations. Thus, for at least the foregoing reasons, none of the cited references, separately or combined, teach or suggest all of the elements of Claim 5.

Huang does not cure the defect of El Gamal. The Examiner cites Huang for disclosing a method of producing thicker and thinner gate oxides. However, Huang also does not teach or suggest each pixel in a pixel array includes a drive transistor, a select transistor, a transfer transistor and a reset transistor, wherein the transistors of the pixel array are based on the first and the second gate insulator layers, and at least one transistor in a logic circuit is based on the second gate insulator layer. Thus, Rhodes in view of El Gamal and Huang does not teach or suggest each of the elements of amended Claim 5.

Claims 12 and 13 depend from Claim 5 and incorporate the limitations thereof. Thus, for at least the reasons mention above, Rhodes in view of El Gamal and Huang does not teach or suggest each of the elements of these dependent claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 5, 12, and 13 are request.

B. Claims 7-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhodes in view of El Gamal and Huang as applied to Claim 5 above, and further in view of Ahn (U.S. Patent No. 5,804,491). Applicants respectfully traverse the rejection.

Claims 7-9 depend from Claim 5 and incorporate the limitations thereof. Thus, for at least the reasons mention above, Rhodes in view of El Gamal and Huang does not teach or suggest each of the elements of these dependent claims.

The Examiner cites Ahn for disclosing a method of removing a gate insulator by wet etching with HF or BOE. However, Ahn does not teach or suggest a pixel array having a number of pixels, each pixel containing a drive transistor, a select transistor, a transfer transistor and a reset transistor, wherein the transistors of the pixel array are based on the first and the second gate insulator layers and at least one transistor in the logic circuit is based on the second gate insulator layer. Thus, none of the cited references teach or suggest each of the elements of Claims 7-9. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 7-9 are requested.

C. Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhodes in view of El Gamal and Huang as applied to Claim 5 above, and further in view of Hori et al. (U.S. Patent No. 5,707,487). Applicants respectfully traverse the rejection.

Claims 10 and 11 depend from Claim 5 and incorporate the limitations thereof. Thus, for at least the reasons mention above, Rhodes in view of El Gamal and Huang does not teach or suggest each of the elements of these dependent claims.

The Examiner cites Hori for disclosing a method of removing a mask using sulfuric acid or an O2 plasma etch. However, Hori does not teach or suggest a pixel array having a number of pixels, each pixel containing a drive transistor, a select transistor, a transfer transistor and a reset transistor, wherein the transistors of the pixel array are based on the first and the second gate insulator layers and at least one transistor in the logic circuit is based on the second gate insulator layer. Thus, none of the cited references teach or suggest each of the elements of Claims 10 and 11. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 10 and 11 are requested.

## II. Allowable Subject Matter

Applicants note with appreciation the Examiner's indication that Claim 6 would be allowable if rewritten in independent form. Applicants respectfully submit that the amendment to Claim 5 has obviated the need to rewrite Claim 6. As Claim 5 is in condition for allowance, Claim 6 is allowable at least for the reasons mentioned in regard to Claim 5. Accordingly, reconsideration and withdrawal of the objection of Claim 6 are requested.

## CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentability define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

Respectfully submitted,

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Date: 2/28/06

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